AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method of forming a bit line contact structure, comprising:

providing a substrate with a transistor, including a gate electrode and a source/drain region thereon, formed on a surface of the substrate, wherein the gate electrode ~~being~~ is protected with a first insulating layer;

conformally forming a titanium layer on the substrate ~~with the transistor thereon~~ to fully and directly cover the transistor and the surface uncovered by the transistor;

conformally forming a titanium nitride layer on the titanium layer;

conformally forming a tungsten layer on the titanium nitride layer;

defining the tungsten layer, the titanium nitride layer and the titanium layer to form an inner landing pad [[on]] conformally and directly covering the source/drain region and a sidewall of the transistor;

conformally forming a passivation layer on the inner landing pad, the transistor and the substrate;

forming a second insulating layer with an even surface on the passivation layer;

forming a contact hole in the second insulating layer and the passivation layer to expose the inner landing pad; and

filling a metal material in the contact hole.

Claim 2 (original): The method of claim 1, wherein a thickness of the tungsten layer is 200-400 Å.

Claim 3 (original): The method of claim 1, wherein the tungsten layer is defined by dry etching.

Claim 4 (original): The method of claim 3, wherein the tungsten layer is dry etched with $Cl_2/F_2/O_2$.

Claim 5 (original): The method of claim 1, wherein the tungsten layer is defined by wet etching.

Claim 6 (currently amended): The method of claim 5, wherein the tungsten layer is wet etched with an APM solution (NH_4OH-H_2O_2-H_2O) at about 40°C.

Claim 7 (original): The method of claim 1, wherein the passivation layer comprises silicon nitride.

Claim 8 (original): The method of claim 1, wherein the passivation layer has a thickness of 110-130 Å.

Claim 9 (original): The method of claim 1, wherein the second insulating layer is a BPSG/TEOS stacked layer.

Claim 10 (currently amended): The method of claim [[1]] 9, wherein a method of forming a BPSG layer of the BPSG/TEOS stacked layer comprises:

depositing a material of BPSG on the passivation layer; and

polishing the material of BPSG until a part of the passivation layer is exposed.

Claim 11 (original): The method of claim 10, wherein the BPSG layer of the BPSG/TEOS stacked layer has a thickness of 5900-7300 Å, and a TEOS layer of the BPSG/TEOS stacked layer has a thickness of 3600-4400 Å.

Claim 12 (original): The method of claim 1, wherein the metal material filled in the contact hole is tungsten.

Claim 13 (original): A method of forming a bit line contact structure on a substrate having a memory array region and a logic circuit region and having a transistor including a gate electrode and a source/drain region thereon, the gate electrode protected with a first insulating layer, the method comprising:

conformally forming a titanium layer on the substrate with the transistor thereon;

conformally forming a titanium nitride layer on the titanium layer;

conformally forming a tungsten layer on the titanium nitride layer;

defining the tungsten layer, the titanium nitride layer and the titanium layer to form an inner landing pad in the memory array region to contact the source/drain region;

conformally forming a passivation layer on the inner landing pad, the transistor and the substrate;

forming a second insulating layer with an even surface on the passivation layer;

forming first, second and third contact holes in the second insulating layer and the passivation layer to expose the inner landing pad in the memory array region, the gate electrode in the logic circuit region and the source/drain region in the logic circuit region respectively; and

filling a metal material in the first, second and third contact holes.

Claim 14 (original): The method of claim 13, wherein a thickness of the tungsten layer is 200-400 Å.

Claim 15 (original): The method of claim 13, wherein the tungsten layer is defined by dry etching.

Claim 16 (original): The method of claim 15, wherein the tungsten layer is dry etched with $Cl_2/F_2/O_2$

Claim 17 (original): The method of claim 13, wherein the tungsten layer is defined by wet etching.

Claim 18 (currently amended): The method of claim 17, wherein the tungsten layer is wet etched with an APM solution (NH_4OH-H_2O_2-H_2O) at about 40°C.

Claim 19 (original): The method of claim 13, wherein the passivation layer comprises silicon nitride.

Claim 20 (original): The method of claim 13, wherein the passivation layer has a thickness of 110-130 Å.

Claim 21 (original): The method of claim 13, wherein the second insulating layer is a BPSG/TEOS stacked layer.

Claim 22 (currently amended): The method of claim 21, wherein a method of forming a BPSG layer of the BPSG/TEOS stacked layer comprises:

depositing a material of BPSG on the passivation layer; and

polishing the material of BPSG until a [[port]] part of the passivation layer is exposed.

Claim 23 (original): The method of claim 22, wherein the BPSG layer of the BPSG/TEOS stacked layer has a thickness of 5900-7300 Å, and a TEOS layer of the BPSG/TEOS stacked layer has a thickness of 3600-4400 Å.

Claim 24 (original): The method of claim 13, wherein the metal material filled in the first, second and third contact holes is tungsten.

Claim 25 (currently amended): A bit line contact structure, comprising:

a substrate;

~~a transistor~~ two adjacent transistors on the substrate, the transistor including a gate electrode and a source/drain region, the gate electrode protected with a first insulating layer;

[[an]] a conformal inner landing pad ~~on a surface~~ formed to fully and directly cover a sidewall of the ~~transistor~~ transistors and the source/drain region between the two adjacent transistors, the conformal inner landing pad comprising a ~~conformal~~ titanium/titanium nitride/ tungsten stacked layer from the bottom up;

a passivation layer on the ~~transistor~~ transistors and the substrate;

a second insulating layer with an even surface on the passivation layer;

a contact plug in the second insulating layer and the passivation layer to contact the inner landing pad; and

an interconnecting landing pad on the contact plug.

Claim 26(original): The bit line contact structure of claim 25, wherein a thickness of the tungsten layer of the inner landing pad is 200-400 Å.

Claim 27 (original): The bit line contact structure of claim 25, wherein the passivation layer comprises silicon nitride.

Claim 28 (original): The bit line contact structure of claim 27, wherein the passivation layer has a thickness of 110-130 Å.

Claim 29 (original): The bit line contact structure of claim 27, wherein the contact plug and the interconnecting landing pad comprises tungsten.